ECS Transactions, 75 (32) 3-12 (2017)
10.1149/07532.0003ecst ©The Electrochemical Society

Control of Resistive Switching in Mott Memories Based on TiN/AM_4Q_8/TiN MIM Devices

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The family of AM_4Q_8 chalcogenide Mott insulators gained attention in recent years for its application opportunities. Here, we explore and validate the resistive switching mechanism of thin-film of GaV_4S_8 sandwiched between TiN electrodes. The device is fabricated via processes and materials compatible with microelectronics standards and demonstrates a good control and endurance of the non-volatile transitions over a large range of resistance. The achieved multi-level property enables to envision application as *Resistive Random Access Memories* (RRAM) or neuromorphic applications. We also showed the important role of the current compliance in the control of the transitions.

Introduction

Memories are at the core of modern digital computation capabilities. During the last decade, significant research efforts have been engaged towards emerging *Non-Volatile Memories* (NVMs). Emerging NVMs, such as *Spin-Torque Transfer Magnetic Random Access Memories* (STT-MRAM) (1, 2), *Phase-Change Random Access Memories* (PCRAM) (3-6) and *Resistive Random Access Memories* (RRAM) (7), exploit the physical properties and electrical behavior of the underlying materials to store a piece of information using other state variable than the electronic charge (8). Relying on unconventional state variables makes NVMs potentially faster, smaller and more robust than current mainstream memory technologies. This work focuses on the RRAM technology where the information is stored by the resistance levels of a material sandwiched between two metal electrodes.

Resistive switching can be achieved through three main classes of physical phenomena (9): (i) ionic migration which is exploited in *Conductive-Bridging Random Access Memories* (CBRAM) (cationic migration) and *Oxide-based Resistive Random Acces Memories* OxRAM (anionic migration); (ii) thermochemical reactions (NiO); and (iii) electronic effects such as the Mott *Metal-Insulator-Transition* (MIT) used in Mott memories. Chalcogenide Mott insulators AM_4Q_8 (A=Ga, Ge; M=V, Nb, Ta; Q=S, Se)

belong to this class of active materials for Mott memories. Data is stored using a new mechanism of resistive switching based on the Mott MIT. Application of electric pulses in these compounds induces an electric-field driven *Resistive Switching* (RS) which originates from an avalanche phenomenon (10). Depending on the strength of the applied electric field, the RS is either volatile or non-volatile (11, 12). While the volatile transition mechanisms have been observed and extensively studied in bulk crystals (10, 12, 13), the mechanisms involved in the non-volatile transition are less understood. Recent results, achieved on AM_4Q_8 – GaV_4S_8 crystals, indicate that the non-volatile transition originates from a stabilization of the volatile transition (14). In particular, these results suggest that a good RS control can be achieved by an alternation of short/high-voltage multi-pulses with long/low-voltage pulses. In addition, they emphasize the significance of current compliance, achieved through a variable resistive load, to better discriminate the mechanisms at work between the set transition, i.e., an electronic avalanche breakdown leading to the local collapse of the Mott insulating state, and the reset transition, i.e., a destabilization of the metastable correlated metallic state by Joule heating. These results also suggest that the load resistance enables to precisely control the physical dimensions of the conductive filaments in the material and achieve intermediate resistance levels between the standard binary levels.

In this paper, we focus on the control of the non-volatile Mott transition for a wide range of values measured on a TiN/GaV_4S_8/TiN thin film device. The geometry and the fabrication process make the devices suited to microelectronics applications and enable to envision large potential of Mott-based devices for consumer applications.

Device Fabrication and Experimental Setup

With the aim of evaluating the RS in Mott insulators within a microelectronics framework, we developed a GaV_4S_8 -based memory technology mostly compatible with materials and processes used in microelectronics. The device consists in a TiN/GaV_4S_8/TiN stack, as shown in Fig. 1-a. Low-temperature sputtered TiN has been used as electrode material for its compatibility with the *Back-End-of-Line*, as it is a common diffusion barrier layer for the metal lines. A 215 nm GaV_4S_8 film is then deposited by reactive magnetron sputtering in a H_2S/Ar plasma with 0.6 % of H_2S. Full details concerning thin film deposition and annealing can be found in literature (15). Fig. 1-b shows the good quality of the TiN/GaV_4S_8 interface since no amorphous region is observed in the continuity of TiN and GaV_4S_8 atomic planes. The patterned passivation layer is realized by lift-off of evaporated Al_2O_3 film of 100 nm. The patterned holes of 2 µm in diameter define the geometry of the device. The top TiN electrode metal is then sputtered and the final top contacts are patterned using optical lithography. The experimental setup used for the electrical tests is depicted in Fig. 1-c. It consists of an Agilent 81150A pulse generator placed in series with a load resistor and the device. The load resistor plays the role of current compliance and, in the context of microelectronics, can be easily realized by a properly biased access transistor. Gold wires connected using carbon paste ensure the electrical contact to the TiN electrodes. Between the applications of programming pulses, the sample resistance is measured at low bias (10 mV) by a Keithley 6430 source-measure unit via a parallel circuit. The fabricated devices have a pristine resistivity of the order of 10 Ω.cm, that is coherent with previous experimental results measured on GaV_4S_8 crystals (16). This guarantees the good crystallinity of the

deposited thin films, as any variation on the stoichiometry would lead to lower resistivity values (17).

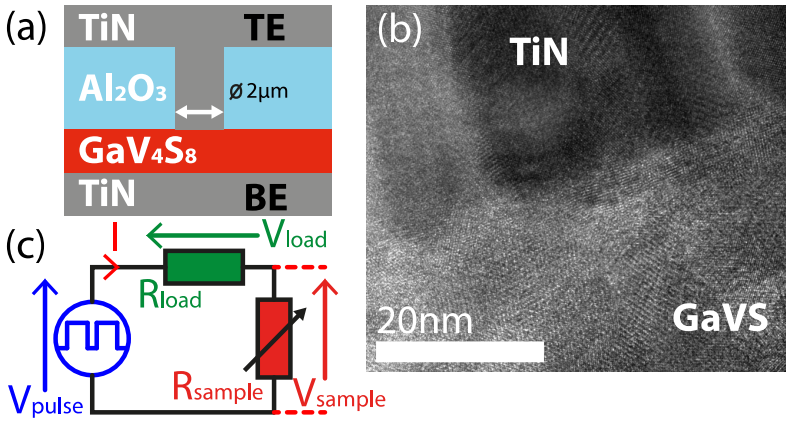

Figure 1. (a) TiN/GaV_4S_8/TiN device stack. Patterned plug in Al_2O_3 is used to define the geometry of the memory. (b) TEM cross-section of the TiN/GaV_4S_8 interface showing a quality interface between the materials and the polycrystallinity of the GaV_4S_8 layer. (c) Experimental setup used for the application of pulses to the sample, which is placed in series with a load resistance and a voltage pulse generator.

Electrical Characterization

The memory characteristics are studied by applied sequences of pulsed signals. We first study the fundamentals of the switching properties of the memory and then we evaluate the impact of the current compliance.

GaV_4S_8 thin-film Switching Mechanism

Microscopic Mechanism of Resistive Switching and Pulse Protocol for the Set and Reset. The electric-field driven volatile transition which appears in GaV_4S_8 single crystals above a threshold electric field E_{th} of a few kV/cm is related to an electronic avalanche effect. Based on our previous simulation works, (18, 19) this volatile transition can be described in terms of collapse of *Mott Insulating* (MI) sites into *Correlated Metallic* (CM) sites. This leads, under a voltage excitation, to the creation of a filamentary percolating path of CM sites in a MI matrix. Our works on bulk GaV_4S_8 crystals have shown that this volatile property can be stabilized into a non-volatile one. The change from the volatile to the non-volatile regime is ascribed to the growth of the conducting filament above a critical diameter under voltage (14). After the pulse application, the conducting filaments are no longer fully percolating but consist in residual granular metallic filamentary paths made of correlated metal domains of a few tens of nanometers embedded in a pristine-like matrix (12, 20, 21). As a consequence the resistance after the pulse is slightly higher than the resistance measured during the pulse. According to our experimental and simulation works, the set transition from the high to the low resistance state is therefore driven by the creation of CM sites under electric field. This can be done either by increasing the voltage pulse well above the threshold field (single-pulse protocol) (16) or by applying several times a lower voltage pulse triggering

the volatile transition (multi-pulse protocol) (14). Conversely, our works suggest that the reset transition is driven by a thermally activated destabilization of the metastable CM sites into MI sites which leads to the dissolution of the conducting filament. For the reset transition, long pulses of low voltage are therefore applied to the material to favor the Joule self-heating effect of the conducting filament. Based on these statements, the pulse protocol designed to switch back and forth on bulk crystals between high and low resistance states is therefore an alternation of moderate voltage multi-pulses with long low voltage pulses. In the present study, we have extended the use of this pulse protocol to thin-film Mott system as illustrated in Fig. 2.

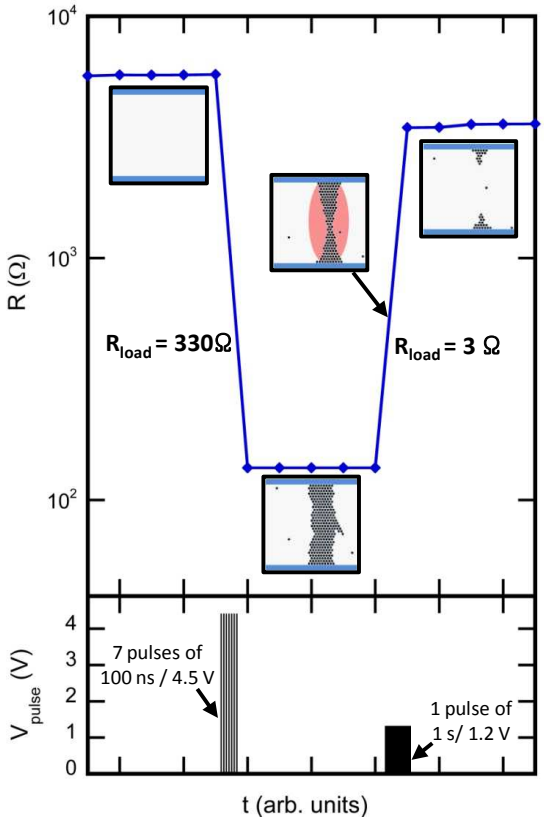

Figure 2. Evolution of the device stack resistance under the application of different series of pulses. Set transition is controlled by a sequence of a multi-pulse of 4.5 V / 7 x 100 ns, while the reset transition is controlled by a single pulse of 1.2 V / 1 s.

Set Transition From the Pristine to a Low Resistance State. We first start with a pristine device whose resistance is 6 kΩ. As schematized in the inset of Fig. 2, the Mott insulating material does not contain CM sites. Starting from this initial state, we have then induced a non-volatile set transition by applying a first sequence of 7 pulses of 100 ns each and separated by 700 ns with a 4.5 V amplitude. A load resistance of 330 Ω is connected in series with the device and serves as a current compliance device. Following the application of the pulse sequence, a transition from the initial high resistance state to a low resistance state of 135 Ω is observed. This phenomenology is in accordance with our previous works on crystals. As illustrated by the inset schemes of Fig. 2, this set transition can be attributed to the creation of a CM filament in a matrix of MI sites. The 330 Ω load resistance aims at limiting the current through the filament and thus at

restricting the Joule heating effect that could compete with the creation of CM sites via their thermal collapse.

Reset Transition From a Low Resistance State to a High Resistance State. Proceeding from this low resistance state (135 Ω), a pulse of 1s with a 1.2 V amplitude is applied to the device, while the load resistance value is lowered to 3 Ω. The application of this pulse leads to a reset transition towards a much higher resistance state of 3500 Ω. This final resistance value is of the same magnitude as the pristine one. It suggests that the Joule self-heating effect of the filament, that is not limited by the load resistance in this case, may have led to its substantial dissolution, as schematized by the inset of Fig. 2. This result also demonstrates that our previous works on the RS control via an optimized pulse protocol in GaV_4S_8 bulk crystals (14) can be transposed to GaV_4S_8 thin films. It must be noted that the long pulse duration of 1 s can probably be reduced by optimizing the thermal design of the device, e.g., reduction of the electrode surface or thermal insulation of memory cells.

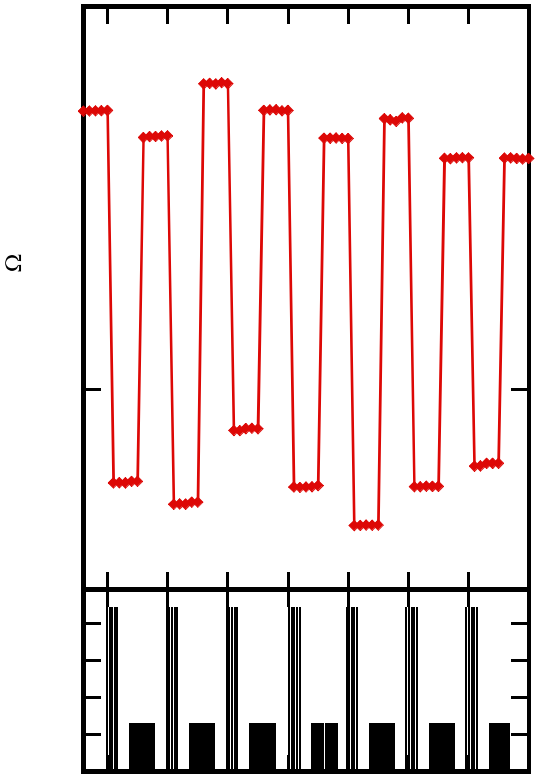

Figure 3. Multiple cycles of set and reset transitions illustrating an achievable R_{OFF}/R_{ON} ratio of 10 with a good stability.

Cycling Between High and Low Resistance States. This mechanism-inspired pulse protocol, consisting in alternating short multi-pulses of high voltage (Set transition) with long single pulses of low voltage (Reset transition), along with the adaptation of the load resistance, enables to switch back and forth reproducibly between a pristine-like resistance state and a low resistance state, as shown in Fig. 3. The average R_{OFF}/R_{ON} ratio measured with this improved pulse protocol reaches a value of 10, which is doubled

compared to our previous results obtained in a similar geometrical configuration with 2 µm-diameter electrodes (22).

Impact of Current Compliance and Multi-level Switching

Multi-level switching is of great interest to achieve both high-density memory applications with multi-bit storage, but also neuromorphic applications. In particular, recent works have shown that the memristive behavior found in most RRAM materials can be used to implement artificial synapses (23). In this section, we will give insights on how intermediate resistance levels can be obtained in the considered Mott Insulator device. For both set and reset transitions, the key tuning parameter is the control of current, implemented through a load resistance in series with the sample.

Control of Current Compliance during Reset : Partial Dissolution of the Filament. Fig. 4 illustrates the impact of the current compliance on the reset transition. Load resistances of 33 Ω and 3 Ω respectively are used. We observe that, following the application of the reset pulse of 1.2 V during 1 s, the resistance state increases to a level that is controlled by the load resistance. Using a low load resistance, it is almost possible to reach back the pristine like resistance state, due to the almost complete dissolution of the conductive filament by Joule heating according to our model. However, a higher load resistance (33 Ω) leads to a lower resistance increase due to the RESET pulse.

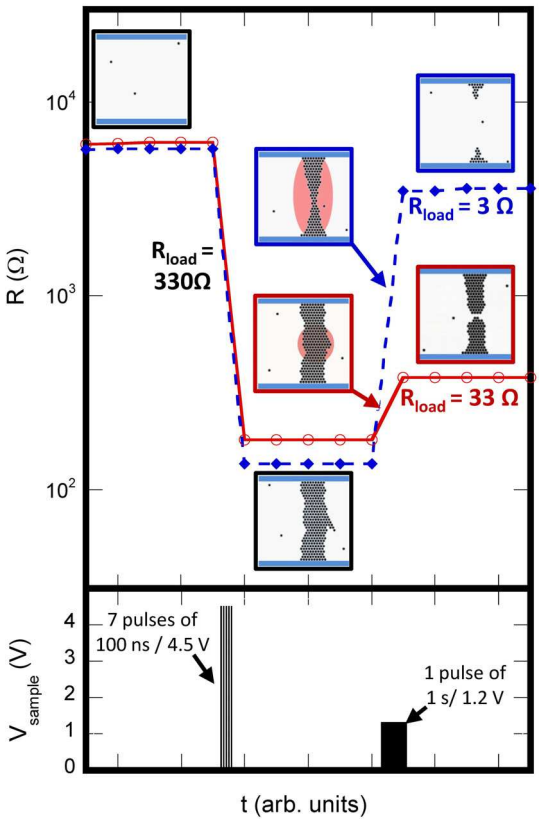

Figure 4. Effect of current compliance on the reset transition. The adaptation of the load resistance, i.e., the current compliance, control the intermediate resistance level.

Once again, our model of resistive switching can give an insight to try and understand this phenomenon. Under voltage a decrease of the sample resistance is observed, which may be ascribed to a change from a granular to a fully percolating metallic state within the filamentary path. Typically a resistance drop by a factor 2 is frequently observed. Due to this sample resistance decrease, the load resistance plays the role of current limiter.

For such a resistance drop by a factor 2, a simple calculation shows that the temperature rise due to Joule heating is reduced by 30 % by changing R_{load} from 3 to 33 Ω. In the case of the higher load resistance (33 Ω) this results in an intermediate resistance state (380 Ω) that may be ascribed to a partial dissolution of the conductive filament.

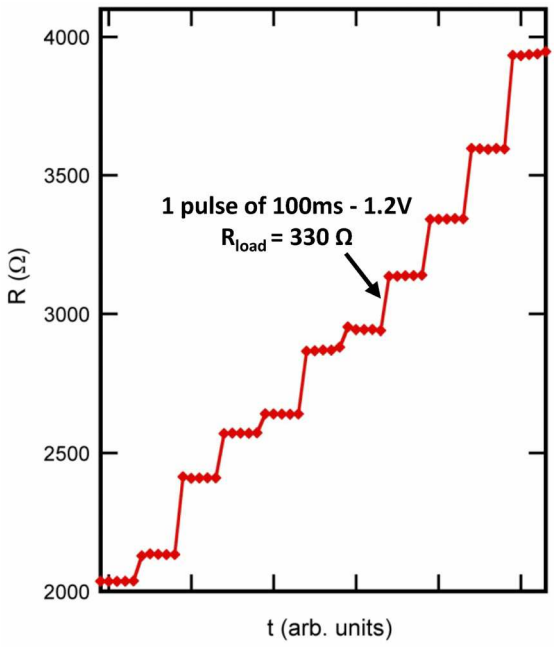

Figure 5. Control of the intermediate resistance levels achievable from successive reset pulses.

Using an intermediate load resistance ranging between 33 Ω and 3 Ω leads to a resistance state intermediate between 380 Ω and the high resistance state. For instance, with a R_{load} of 10 Ω, an intermediate resistance level of about 2 kΩ is reached. This clearly suggests that, depending on the conditions used for the reset, the conducting filamentary path can be more or less broken and eroded.

Alternatively, using successive reset pulses with lower duration, it is also possible to control intermediate resistance levels with a very fine granularity. As illustrated in Fig. 5, starting from an intermediate resistance state of about 2 kΩ, the application of 100ms / 1.2 V pulses allows us to increase the resistance step by step toward the high resistance state. Again, this may be related to the gradual destruction of the conducting filamentary path. Fig. 5 achieves a total of 11 different states, which would enable the storage of more than 3 bits of information in a single node.

Control of Current Compliance during Set: Partial Reconstruction of the Filament

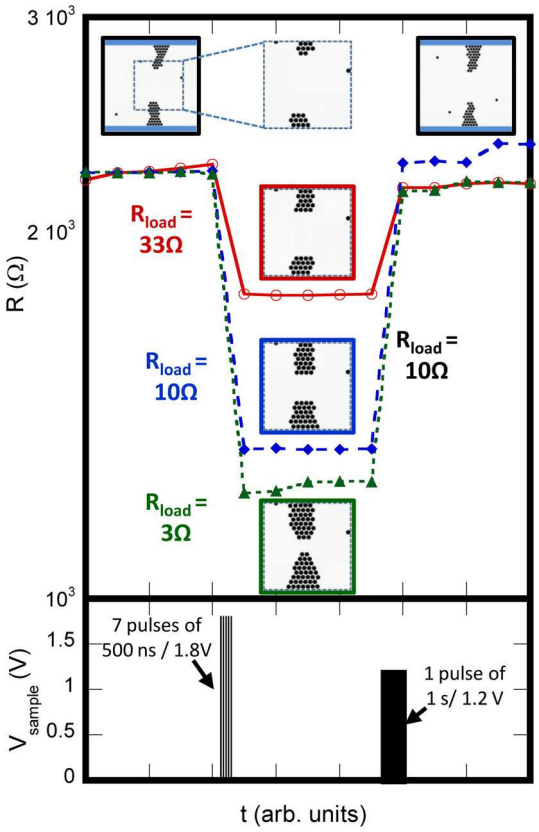

Figure 6. Impact of current compliance on the set transition obtained with different values of R_{load} 3 Ω, 10 Ω and 33 Ω respectively.

Fig. 6 demonstrates that, starting from an intermediate resistance level of about 2 kΩ, new lower intermediate resistance states can be achieved by adjusting the current compliance during the set transition. The application of 7 pulses of 500 ns / 1.8 V every 3.5 µs with load resistances of 3 Ω, 10 Ω and 33 Ω triggers a resistive switching from 2.4 kΩ to 1.23 kΩ, 1.33 kΩ and 1.78 kΩ respectively. Again, this might be understood in the framework of our model, as illustrated in the insets of Fig. 6. With our setup, decreasing the load resistance value during the set induces an enhancement of the current during the pulse. The self stabilization of the voltage at the threshold during the pulse implies that the current directly controls the metallic filamentary path conductance and thus the quantity of CM sites needed to rebuild the filamentary path. The choice of set conditions allows therefore controlling the partial reconstruction of the broken conducting filament and the level of intermediate resistance. This scenario is sketched on the insets of Fig. 6, hypothesizing that the broken part is located at the middle of the filament. However it must be noted that at this stage of our understanding, the precise location of the filament broken part (i.e., close to the electrodes or in the middle of the filament) is unknown.

Cycling Between Intermediate States

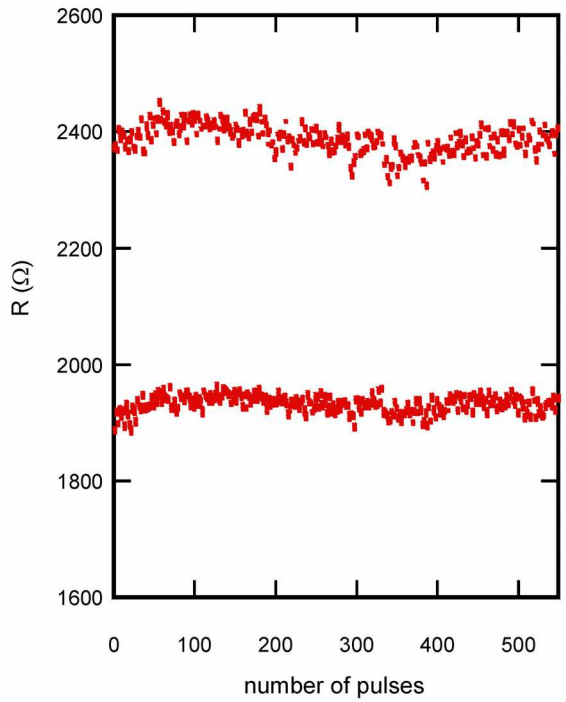

Figure 7. Resistive switching cycles obtained on the considered device, showing good device endurance and stability of the resistance window.

An important issue of the multi-bit storage is to achieve a reproducible cycling between intermediate resistance states. We subsequently focused on the endurance properties of the memory node between two arbitrarily chosen intermediate states. Therefore, we stressed the memory with series of set and reset pulse sequences, similar to the ones used in Fig. 6. As demonstrated in Fig. 7, each pulse induces a systematic transition between intermediate high and low resistance states, with a very low variability and no degradation after few hundreds of cycles.

Conclusion

We demonstrated a good control of the non-volatile transition in a thin-film of GaV_4S_8 sandwiched between TiN electrodes. The device is fabricated via processes and materials targeting microelectronics standards. A control of the transition over a large range of resistance is achieved, thus enabling to envision application as RRAM but also neuromorphic applications. We also showed the important role of the current compliance in the control of intermediate resistance states.

Acknowledgement

This work was supported by the Swiss National Science Foundation (FNS) grant 200021-122168 and French Agence Nationale de la Recherche (ANR) grant `Mott-RAM' (ANR-2011-EMMA-016-01).

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